Displaying records # 1 through 7 out of 7

Result # 1 Relevance:

Advanced Header Splitting Buffer Management

17-Jul-2002 IPCOM000008840D English (United States)

Disclosed is a method that enables an I/O controller to determine buffer usage based on packet size. The disclosed method also minimizes the use of oversized receive buffers to handle minimal amounts of traffic. Benefits include better memory management and less buffer ...

Result # 2 Relevance:

Autonomic Buffer Pool Management to improve sequential read and write I/O performance

2006-07-18 IPCOM000138459D English (United States)

Disclosed is an autonomic buffer pool management which exploits additional prefetch buffers only when a good improvement is expected and avoid overall system performance regression from an excessive use of buffer resource. This becomes more critical, and beneficial, as ...

Result # 3 Relevance:

patents

1990-05-31 IPCOM000163786D English (United States)

by the U.S. Patent Ofice are reproduced exactly as they appear on the original published patent. Thefoilowing patents were recently issued by the countries in which the inventions were made. For U.S. patents, titles and names supplied to US United States 4,796,206 ...

Result # 4 Relevance:

Method for a memory coprocessor to prefetch objects

20-Nov-2002 IPCOM000010334D English (United States)

Disclosed is a method for a memory coprocessor to prefetch objects. Benefits include improved functionality.

Result # 5 Relevance:

Utilization-Based Prefetching

1985-02-01 IPCOM000063165D English (United States)

Utilization properties are used to prefetch units of blocks in a memory hierarchy comprised of three levels: a main memory at level 3 (L3), a second level cache (L2) and a first level cache (L1). In computer storage hierarchies (e.g., caches, memories) the ...

Result # 6 Relevance:

Managing IBM Database 2 buffers to maximize performance

1984-06-30 IPCOM000164933D English (United States)

The relational data base system, IBM Database 2(DB2), has a component that manages data buffering. This paper describes the design considerations of the Buffer Manager and the tradeoffs involved in managing the allocation of DB2 buffers to maximize performance. Data base ...

Result # 7 Relevance:

Adaptive Variation of the Transfer Unit in a Storage Hierarchy

1978-07-31 IPCOM000163218D English (United States)

P. A. Franaszek B. T. Bennett Adaptive Variation of the Transfer Unit ina Storage Hierarchy Abstract: Consider a paged storage hierarchy with at least two levels L, and L,, where L, denotes main storage and Lz secondary storage. Suppose that the unit of replacement ...

Search query: **prefetch* w/30 threshold**

New search | Modify this search | Search within current results

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Result # 1 Relevance:

Cache Miss Director - A Means of Prefetching Cache Missed Lines

1982-08-01 IPCOM000050035D English (United States)

In a computing system with a cache, when the CPU encounters a storage reference that cannot be satisfied by the cache (a demand miss), processing usually must be delayed for an access to main storage. Because of the increasing disparity between CPU and main storage speeds, ...

Result # 2 Relevance:

Method for the hot stack coprocessor

02-May-2002 IPCOM000007897D English (United States)

Disclosed is a method for the hot stack coprocessor. Benefits include improved functionality and improved performance.

Result # 3 Relevance:

Method for stride-profile guided prefetching for irregular code

16-Jun-2004 IPCOM000029128D English (United States)

Disclosed is a method for stride-profile guided prefetching for irregular code. Benefits include improved functionality and improved performance.

Result # 4 Relevance:

abstracts

1993-11-30 IPCOM000163993D English (United States)

Abstracts 1957-1993 Volume 1, Number 1, 1957Domain Orientation in Barium Titanate Single Crystals by D. P. Cameron, p. 2. An acid etching technique makes visible the domain structure of barium titanate crystals as reported by Hooton and Merz . Earlier observations by Merz ...

Result # 5 Relevance:

EVALUATION OF A DECOUPLED COMPUTER ARCHITECTURE AND THE DESIGN OF A VECTOR EXTENSION

1985-05-31 IPCOM000161115D English (United States)

EVALUATION OF A DECOUPLED COMPUTER ARCHITECTURE ANDTHE DESIGN OF A VECTOR EXTENSION HONESTY CHENG YOUNG Computer Sciences Dep clrtmen t University of Wisconsin-Madison Madison, WI 53706 May 1985 to my Parentsfor their love, faith, support, encouragement, and ...

Result # 6 Relevance:

Predicting the performance of distributed virtual shared-memory applications

1997-12-31 IPCOM000165451D English (United States)

K. C. Sevcik The use of networks of workstations for parallel computing is becoming increasingly common. Networks of workstations are attractive for a large class of parallel applications that can tolerate the higher network latencies andlower bandwidth associated with ...

Result # 7 Relevance:

A STRUCTURED MEMORY ACCESS ARCHITECTURE FOR LISP

1986-08-31 IPCOM000161083D English (United States)

by MATTHEW JACOB THAZHUTHAVEETIL A thesis submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy (Computer Sciences) at the UNIVERSITY OF WISCONSIN-MADISON August 1986 A STRUCTURED MEMORY ACCESS ARCHITECTURE FOR LISP ...

Result # 8 Relevance:

POINTWISE CONTRACTION CRITERIA FOR THE EXISTENCE OF FIXED POINTS

1976-07-31 IPCOM000152125D English (United States)

A STRUCTURED MEMORY ACCESS ARCHITECTURE FOR LISP by MATTHEW JACOB THAZHUTHAVEETIL A thesis submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy (Computer Sciences) at the UNIVERSITY OF WISCONSIN-MADISON August 1986 A ...

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Search query: (prefetch* w/30 (cache w/5 miss*)) and threshold

New search | Modify this search | Search within current results

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Result # 1 Relevance:

Method for hardware prefetching of the structured data of cache miss loads

17-Aug-2005 IPCOM000127016D English (United States)

Disclosed is a method for hardware prefetching of the structured data of cache miss loads. Benefits include improved functionality and improved performance.

Result # 2 Relevance:

Instruction Cache Miss State Machine and Cache Miss Request

1989-07-01 IPCOM000035314D English (United States)

A common approach to providing instructions for pipelined processors to minimize the instruction wait time is to prefetch instructions. When a cache miss occurs on an address that corresponds to a prefetched instruction, the processor may or may not actually need that ...

Result # 3 Relevance:

Prefetching Pacing Buffer to Reduce Cache Misses

1984-10-01 IPCOM000043872D English (United States)

To reduce the occurrence of memory subsystem lockouts caused by excessive prefetching of instruction lines, a bit in each prefetch target line is used as a tag that is set if a prefetch of that line takes place in the same interval that a cache miss occurs. Tagged lines then ...

Result # 4 Relevance:

Algorithm for Non-Sequential Cache Prefetching

1991-07-01 IPCOM000121106D English (United States)

Disclosed is an algorithm for initiating cache prefetches for data to potentially non-sequential cache lines, based on the past history of cache misses.

Result # 5 Relevance:

A METHOD FOR CACHE MANAGEMENT IN STORAGE SYSTEMS

2004-02-18 IPCOM000021984D English (United States)

The invention described here is a method and a system for maintaining a so-called "value function" which assigns a numercial value to any feasible cache contents with respect to past statistics of data accesses. This function is used for deciding how to dynamically ...

Result # 6 Relevance:

a load-instruction unit for pipelined processors

1993-07-31 IPCOM000163974D English (United States)

instruction unit for pipelined processors A special-purpose load unit is proposed aspart of a processor design. The unit prefetches data from the cache by predicting the address of the data fetch in advance. This prefetch allows the cache access to take place early, in an ...

Result # 7 Relevance:

Cache Miss Director - A Means of Prefetching Cache Missed Lines

1982-08-01 IPCOM000050035D English (United States)

In a computing system with a cache, when the CPU encounters a storage reference that cannot be satisfied by the cache (a demand miss), processing usually must be delayed for an access to main storage. Because of the increasing disparity between CPU and main storage speeds, ...

Result # 8 Relevance:

prefetching and memory system behavior of the SPEC95 benchmark suite

1997-05-31 IPCOM000164190D English (United States)

Prefetching and memory system behaviorof the SPEC95 benchmark suite I . This paper presents instruction and data cache miss rates for the SPEC95* benchmark suite. We have simulated the instruction and data traffic resulting from 500 million instructions of each ...

Result # 9 Relevance:

improving performance of linear algebra Al Gore rhythms for dance matrices, using algorithmic prefetch

1994-05-31 IPCOM000164011D English (United States)

In this paper, we introduce a concept called algorithmic prefetching, for exploiting some of the features of the IBM RISC System/6000@* computer. Algorithmic prefetching denotes changing algorithm A to algorithm B, which contains additional steps to move data from slower ...

Result # 10 Relevance:

Burst-Controlled Prefetching to Reduce Finite Cache Penalty

1983-11-01 IPCOM000047504D English (United States)

To reduce the finite cache penalty in memory systems having variable-length lines, it is proposed to control the prefetching process in such a way that the shorter lines are prefetched during bursts of cache misses and the longer lines are prefetched during the gaps between ...

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Search query: prefetch* w/30 (cache w/2 miss*)

New search | Modify this search | Search within current results

Displaying records # 1 through 2 out of 2

Result # 1 Relevance:

Page Allocation Control

1990-01-01 IPCOM000099270D English (United States)

Disclosed is a method to improve the cache hit of a computer system by controlling the physical page using the activity monitoring circuit. This is effective in the systems with both demand paging a direct-mapped (one way associative), large, physical cache. (Image ...

Result # 2 Relevance:

A Methodology for Adaptive Cache Size Management using Set-Associative Metrics

2003-06-18 IPCOM000013472D English (United States)

Described is an adaptive methodology for adjusting cache sizes for optimum application execution, with a specific focus on set-associative metrics.

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Search query: replac* w/30 cache w/30 threshold

New search | Modify this search | Search within current results